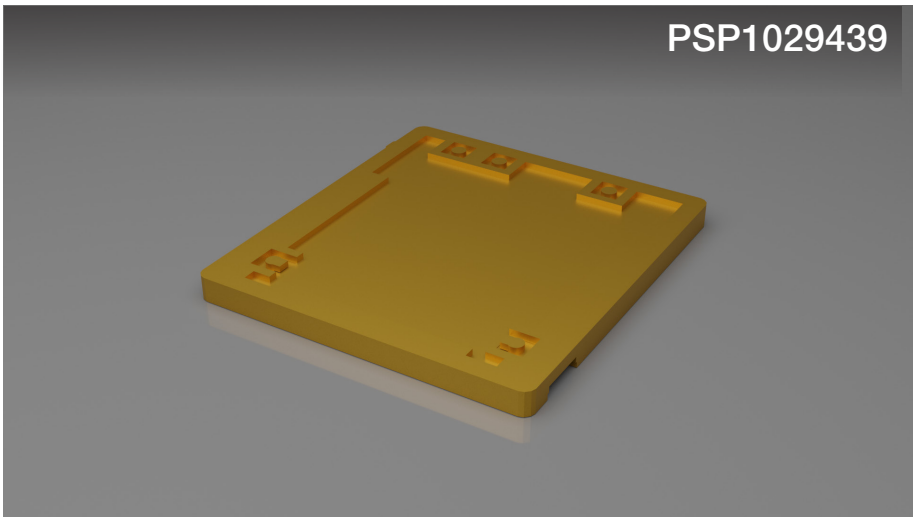
Features and Benefits

- Optimized package for Qorvo's TGA2962
- Efficient heat removal through package lid
- Chip interface compatible with automated Au wire bonding
- PCB interface compatible with standard SMT processes



Applications

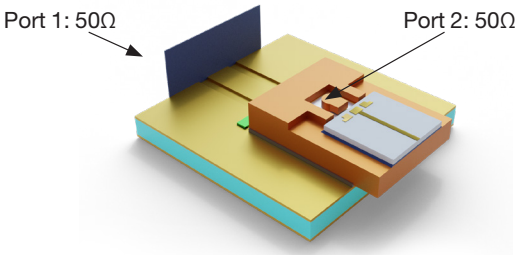
- Military
- Space
- Communications
- Instrumentation

PolyStrata® Package: PSP1029439

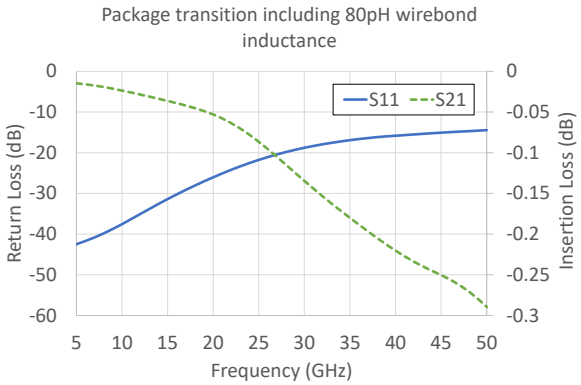
Air-Cavity package optimized for the Qorvo's TGA2962 2-20 GHz 10 Watt GaN Amplifier.

Nuvotronics presents a state of the art package optimized for the TGA2962 from Qorvo. Maintains the performance of the TGA2962 die but in an easy to use SMT compatible device. Compared to the QPA2962, this package enhances thermal spreading of heat from the die and enables efficient removal of heat through the top and sides of the package, eliminating the need for thermal path through the PCB. The package is 5.5 x 6 x 1.45mm including the matched metal lid with adequate internal space to include 820 pF wire bonded capacitors for increased stability.

Typical Electrical Performance



P1 is on the PCB with reference plane de-embedded to the edge of PolyStrata package. P2 is on the PolyStrata wire bonding pad. To approximate the wire bonds, an 80pH inductance is included in the plot for Return Loss and Insertion Loss (right figure).



Additional Details

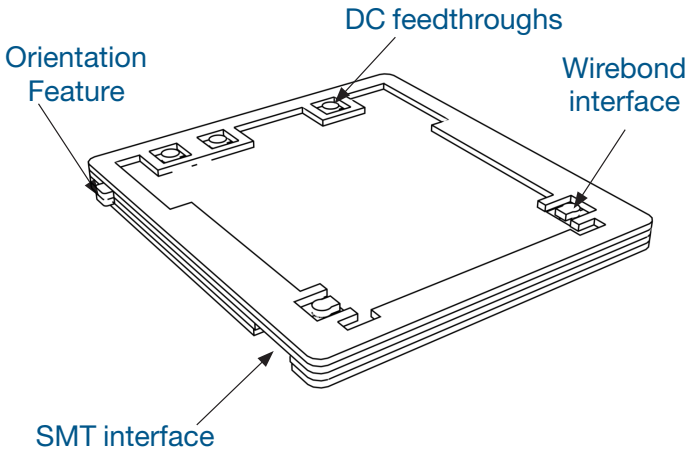
Special Handling / Storage Instructions (Substrate Only)	
Storage	Per JEP160 - Oxygen Sensitive Devices
ESD Sensitivity	None
Moisture Sensitivity	Not Applicable
Component Termination Finish	Immersion Gold over Immersion Silver
Packaging Available	Tape and Reel
Ordering Part Number	PSP1029439
Export Classification	EAR99
Ordering Lid Options	1028940-009

Absolute Maximum Ratings

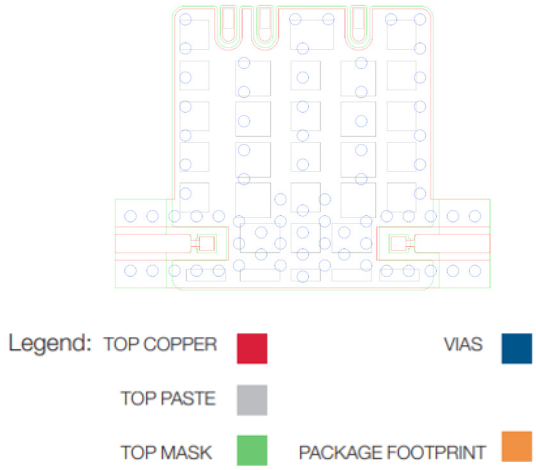
Current	2.0 amps
Operating Temp	-55°C to 125°C
Solder Reflow	Compatible with JEDEC J-STD-020
Epoxy Attach	150°C max. for 90 minutes

PCB Stack-up View

Component View

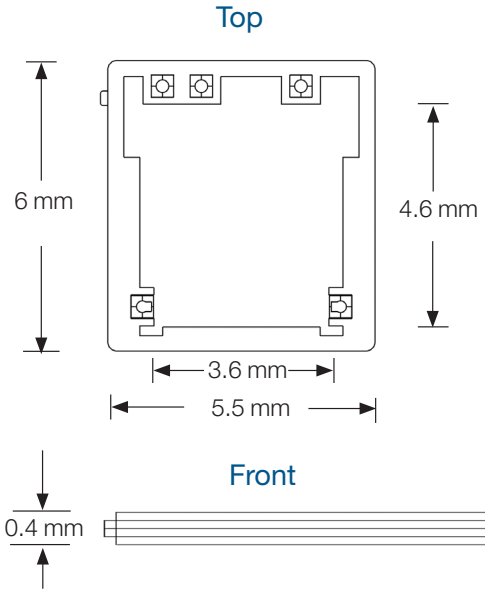


PCB Layout

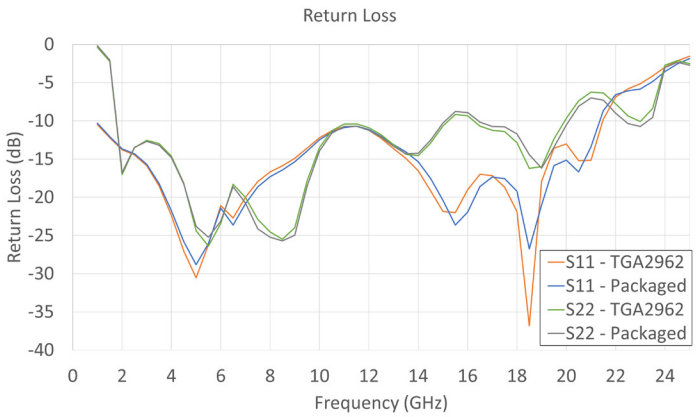


3D models, S-parameters, board footprint
DXF drawings available on request

Mechanical Drawing



Package on Board Vs Bare Die Performance Comparison



Thermal Information

A finite element analysis was conducted to evaluate the thermal performance of the package based on which surface the heat is removed from and the adhesives used in package assembly.

Theta$_{jc}$ (θ_{jc}) represents the thermal resistance in a given scenario, describing the temperature rise between the constant temperature location (heat sink) and the channel temperature of the chip. A lower θ_{jc} indicates more efficient cooling of the chip.

The analysis indicates lower θ_{jc} values when heat is removed from the package base. However, this does not account for the additional thermal resistance from the PCB, which lies between the package and the heat sink. This resistance can vary significantly depending on PCB construction. Conversely, attaching the heat sink directly to the lid is straightforward and eliminates any additional thermal resistances, resulting in lower case temperatures compared to devices cooled through the PCB.

For instance, if the heat sink in contact with the lid is maintained at 25°C, the channel temperature will be 195°C at 45W of dissipated power, when using a silver sinter paste as the adhesive.

Heat Removal Location	Adhesive Material	θ_{jc} (°C/W)
Package Base (PCB side)	Silver Epoxy	2.95
	SN63 Solder	2.74
	Silver Sinter Paste	2.73
Package Lid	Silver Epoxy	4.51
	SN63 Solder	3.84
	Silver Sinter Paste	3.77

Notes:

- Adhesive locations are between the die and package and the package and lid.
- Both locations use the same indicated adhesive as indicated in the table above.
- At both locations the adhesive thickness was assumed to be 12µm.

Cross-Section of FEA Model